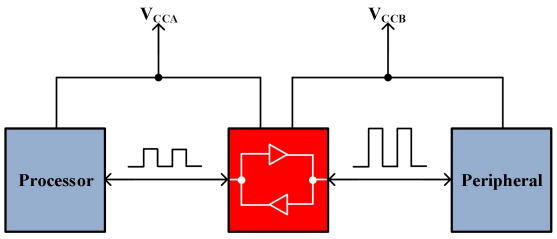
GT0208
8-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing

1 Features	2 Application
- No direction-control - Data rates: 100 Mbps (Push Pull) - 1.2 V to 3.6 V on A ports and 1.65 V to 5.5 V on B ports ($V_{CCA} \leq V_{CCB}$) - V_{CC} Isolation Feature: If either V_{CC} input is at GND, both ports are in the high-impedance state - OE Input Circuit Referenced to V_{CCA} - I_{off} supports partial-power-down mode operation - Operating temperature range:-40℃ to +85℃	- Handset - Smartphone - Tablet - Desktop PC

3 Description	Circuit Diagram
This 8-bit non-inverting decoder is a bi-directional voltage level decoder that can be used to establish digital switching compatibility between mixed voltage systems. It uses two independent, configurable power rails, with port A supporting operating voltages from 1.2V to 3.6V while tracking the V_{CCA} supply, and port B supporting operating voltages from 1.65V to 5.5V while tracking the V_{CCB} supply. This supports both lower and higher logic signal levels and provides bi-directional switching between 1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5V voltage nodes. V_{CCA} must not exceed V_{CCB}. When the output enable (OE) input is low, all outputs are in a high impedance state, which greatly reduces power supply quiescent current consumption. OE has an internal pull-down current source as long as V_{CCA} is powered. The OE has an internal pull-down current source as long as V_{CCA} is powered. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.	

4 Device Summary, Pin and Packages

Table 4-1. Device Summary(1)

Serial Name	Part Name	Package	Body Size (Nom)	Marking(2)	MSL(3)	Package Qty
GT0208	GT0208TG	TSSOP20	6.50mm×4.40mm	GT0208 XXXXXXX	3	Tape and Reel,4000
	GT0208QSG	QFN3×3-20L	3.00mm×3.00mm	GT0208 XXXXX	3	Tape and Reel,5000

(1)For all available packages, please contact product sales.

(2)There may be additional marking, which relates to the lot trace code information (data code and Vendor code), the logo or the environmental category on the device.

(3)MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4)"XXXXX" in Marking will be appeared as the batch code.

4 Device Summary, Pin and Packages(Continued)

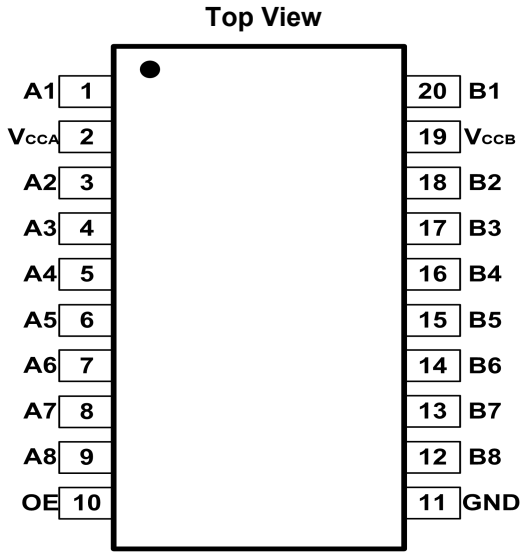


Fig.4-1. GT0208: TG (TSSOP20) Package

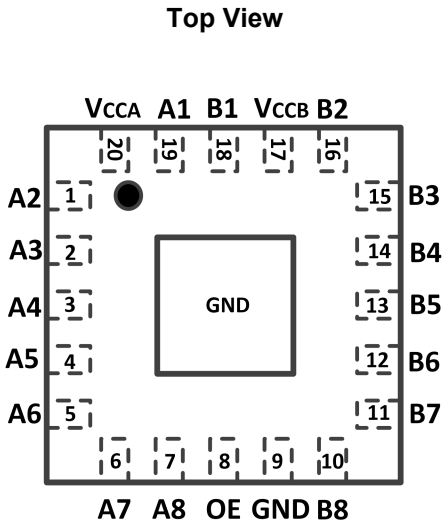


Fig.4-2. GT0208: QSG (QFN3×3-20L) Package

Table 4-2. Pin Definition

Pin			I/O	Function
Name	TG	QSG		
A1	1	19	I/O	Input/Output A1. Referenced to V_{CCA}.
V_{CCA}	2	20	-	A-Port power supply.
A2	3	1	I/O	Input/Output A2. Referenced to V_{CCA}.
A3	4	2	I/O	Input/Output A3. Referenced to V_{CCA}.
A4	5	3	I/O	Input/Output A4. Referenced to V_{CCA}.
A5	6	4	I/O	Input/Output A5. Referenced to V_{CCA}.
A6	7	5	I/O	Input/Output A6. Referenced to V_{CCA}.
A7	8	6	I/O	Input/Output A7. Referenced to V_{CCA}.
A8	9	7	I/O	Input/Output A8. Referenced to V_{CCA}.
OE	10	8	I	Tri-state output mode. Pull low put all outputs in tri-state. Referenced to V_{CCA}
GND	11	9	-	Ground
B8	12	10	I/O	Input/Output B8. Referenced to V_{CCB}
B7	13	11	I/O	Input/Output B7. Referenced to V_{CCB}
B6	14	12	I/O	Input/Output B6. Referenced to V_{CCB}
B5	15	13	I/O	Input/Output B5. Referenced to V_{CCB}
B4	16	14	I/O	Input/Output B4. Referenced to V_{CCB}
B3	17	15	I/O	Input/Output B3. Referenced to V_{CCB}
B2	18	16	I/O	Input/Output B2. Referenced to V_{CCB}
V_{CCB}	19	17	-	B-Port power supply
B1	20	18	I/O	Input/Output B1. Referenced to V_{CCB}

*It is suggested to leave the unconnected pins floating.

5 Voltage, Temperature, ESD and Thermal Ratings

5.1 Absolute Maximum Ratings(1)(2)(3)

Parameters		Min	Max	Unit
Supply voltage, V_{CCA}		-0.3	6.5	V
Supply voltage, V_{CCB}		-0.3	6.5	V
Input voltage range,V_I	A port	-0.3	6.5	V
	B port	-0.3	6.5	
	OE	-0.3	6.5	
Voltage range applied to any output in the high-impedance or power-off state, Vo	A port	-0.3	6.5	V
	B port	-0.3	6.5	
Voltage range applied to any output in the high or low state, Vo	A port	-0.3	V_{CCA}+0.3	V
	B port	-0.3	V_{CCA}+0.3	
Input clamp current,I_{IK}	V_I＜0		-50	mA
Output clamp current,I_{OK}	V_O＜0		-50	mA
Continuous output current,I_O			±50	mA
Continuous current through V_{CCA},V_{CCB} or GND			±100	mA
Maximum junction temperature			150	°C
Storage temperature range		-65	150	°C

(1)Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2)The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed

(3)The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table

5.2 ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic Discharge	Human-Body Model (HBM)(1)	±5K	V
		Charged-Device Model (CDM)(2)	±2K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5 Voltage, Temperature, ESD and Thermal Ratings(Continued)

5.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply Voltage associated with the output port.

Parameter	Conditions			Min	Typ	Max	Unit
Supply voltage (1)	V_{CCA}			1.2		5.5	V
	V_{CCB}			1.65		5.5	
High-level input voltage(V_{IH})	A-port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		V_{CCI}×0.81		V_{CCI}	V
	B-port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		V_{CCI}×0.81		V_{CCI}	
	OE input	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		V_{CCA}×0.65		5.5	
Low-level input voltage(V_{IL})(2)	A-port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		0		V_{CCI}×0.35	V
	B-port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		0		V_{CCI}×0.35	
OE	OE input	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		0		V_{CCA}×0.35	V
Voltage range applied to any output in the high-impedance or power-off state, Vo	A-port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		0		5.5	V
	B port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V		0		5.5	V
Input transition rise or fall rate(Δt/Δv)	A-port I/Os	V_{CCA}=1.2 V to 5.5 V V_{CCB}=1.65 V to 5.5 V				40	ns/V
	B port I/Os	V_{CCA}=1.2 V to 5.5 V	V_{CCB}=1.65 V to 5.5 V			40	
			V_{CCB}=4.5 V to 5.5 V			30	
TA Operating free-air temperature	-			-40		85	°C

(1)V_{CCA} must be less than or equal to V_{CCB}.

(2)The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is V_{IL} plus the voltage drop across the pass gate transistor.

6 Electrical Specifications

6.1 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1) (2) (3)

Parameter		Conditions	VccA	VccB	Temp	Min	Typ	Max	Unit
V_{OHA}	Port A Output High Voltage	I_{OH}=–20 μA	1.2V		+25℃		1.1		V
			1.4V to 5.5V		Full	V_{CCA}-0.4			
V_{OLA}	Port A Output Low Voltage	I_{OL}=20 μA	1.2V		+25℃		0.3		V
			1.4V to 5.5V		Full			0.4	
V_{OHB}	Port B Output High Voltage	I_{OH}=–20 μA		1.65V to 5.5V	Full	V_{CCA}-0.4			V
V_{OLB}	Port B Output Low Voltage	I_{OL}=20 μA		1.65V to 5.5V	Full			0.4	V
I_I	Input Leakage Current	OE I=V_{CCI} or GND	1.2V to 5.5V	1.65V to 5.5V	+25℃			±1	μA
					Full			±2	
I_{off}	Partial Power Down Current	A Ports	0V	0V to 5.5V	+25℃			±1	μA
					Full			±2	
		B Ports	0V to 5.5V	0V	+25℃			±1	
					Full			±2	
I_{OZ}	High-impedance State Output Current	A or B port OE=0V	1.65V to 5.5V	2.3V to 5.5V	+25℃			±1	μA
					Full			±2	
I_{CCA}	V_{CCA} Supply Current	V_I=V_O=open I_O=0	1.2V	1.65V to 5.5V	+25℃		0.06		μA
			1.4V to 5.5V	1.65V to 5.5V	Full			5	
			5.5v	0V	Full			2	
			0v	5.5V	Full			-2	
I_{CCB}	V_{CCB} Supply Current	V_I=V_O=open I_O=0	1.2V	1.65V to 5.5V	+25℃		3.4		μA
			1.4V to 5.5V	1.65V to 5.5V	Full			5	
			5.5v	0V	Full			-2	
			0v	5.5V	Full			2	
I_{CCA} + I_{CCB}	Combined Supply Current	V_I=V_{CCI} or GND I_O=0	1.2V	1.65V to 5.5V	+25℃		3.5		μA
			1.4V to 5.5V	1.65V to 5.5V	Full			10	
I_{CCZA}	V_{CCA} Supply Current	V_I=V_{CCI} or 0V I_O=0, OE=0V	1.2V	1.65V to 5.5V	+25℃		0.05		μA
			1.4V to 5.5V	1.65V to 5.5V	Full			5	
I_{CCZB}	V_{CCB} Supply Current	V_I=V_{CCI} or 0V I_O=0, OE=0V	1.2V	1.65V to 5.5V	+25℃		3.3		μA
			1.4V to 5.5V	1.65V to 5.5V	Full			5	
C_i	Input Capacitance	OE	1.2V to 5.5V	1.65V to 5.5V	+25℃		4		PF
C_{io}	Input-to-output Internal Capacitance	A Port	1.2V to 5.5V	1.65V to 5.5V	+25℃		5		PF
		B Port	1.2V to 5.5V	1.65V to 5.5V	+25℃		9		

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port

(3) V_{CCA} must be less than or equal to V_{CCB}.

6 Electrical Specifications(Continued)

6.2 Timing Requirements

T_A=25℃ (unless otherwise noted)

V_{CCA}=1.2V

		V_{CCB}=1.8V	V_{CCB}=2.5V	V_{CCB}=3.3V	V_{CCB}=5V	Unit
		Typ	Typ	Typ	Typ	
Data Rate		20	20	20	20	Mbps
Pulse Duration(tw)	Data inputs	50	50	50	50	ns

V_{CCA}=1.5V±0.1V

		V_{CCB}=1.8V±0.15V	V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.3V	V_{CCB}=5V±0.5V	Unit
		Typ	Typ	Typ	Typ	
Data Rate		40	40	40	40	Mbps
Pulse Duration(tw)	Data inputs	25	25	25	25	ns

V_{CCA}=1.8V±0.15V

		V_{CCB}=1.8V±0.15V	V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.3V	V_{CCB}=5V±0.5V	Unit
		Typ	Typ	Typ	Typ	
Data Rate		52	60	60	60	Mbps
Pulse Duration(tw)	Data inputs	19	17	17	17	ns

V_{CCA}=2.5V±0.2V

		V_{CCB}=2.5V±0.2V	V_{CCB}=3.3V±0.2V	V_{CCB}=5V±0.2V	Unit
		Typ	Typ	Typ	
Data Rate		70	80	80	Mbps
Pulse Duration(tw)	Data inputs	14	12	12	ns

V_{CCA}=3.3V±0.3V

		V_{CCB}=3.3V±0.3V	V_{CCB}=5V±0.5V	Unit
		Typ	Typ	
Data Rate		80	100	Mbps
Pulse Duration(tw)	Data inputs	12	10	ns

6 Electrical Specifications(Continued)

6.3 Switching Characteristics: V_{CCA}=1.2V

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	V_{ccB}=1.8V	V_{ccB}=2.5V	V_{ccB}=3.3V	V_{ccB}=5V	Units
			Typ	Typ	Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	21.40	20.00	21.20	25.60	ns
t_{PLH}	Propagation Delay Time High-to-low Output	A to B	25.40	20.50	19.60	29.40	ns
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	24.20	21.40	22.10	21.10	ns
t_{PLH}	Propagation Delay Time High-to-low Output	B to A	27.70	25.00	23.30	23.80	ns
t_{en}	Enable Time	OE to A or B	55.90	56.90	57.30	56.10	ns
t_{dis}	Disable Time	OE to A or B	169.90	165.00	167.30	174.00	ns
t_{rA}	Input Rise Time	A port rise time	5.80	5.50	5.00	3.60	ns
t_{rB}	Input Rise Time	B port rise time	9.00	7.70	7.00	7.40	ns
t_{fA}	Input Fall Time	A port fall time	4.00	3.80	4.80	4.80	ns
t_{fB}	Input Fall Time	B port fall time	8.70	7.80	6.00	6.40	ns
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew	0.5	0.5	0.5	0.5	ns
Maximum Data Rate			20	20	20	20	Mbps

6.4 Switching Characteristics: V_{CCA}=1.5V±0.1V

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	V_{ccB}=1.8V±0.15V	V_{ccB}=2.5V±0.2V	V_{ccB}=3.3V±0.3V	V_{ccB}=5V±0.5V	Units
			Typ	Typ	Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	17.30	13.90	13.80	13.50	ns
t_{PLH}	Propagation Delay Time High-to-low Output	A to B	19.90	17.80	16.60	13.15	ns
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	20.40	12.30	11.90	11.80	ns
t_{PLH}	Propagation Delay Time High-to-low Output	B to A	20.60	18.50	17.30	16.20	ns
t_{en}	Enable Time	OE to A or B	41.20	45.30	44.70	51.50	ns
t_{dis}	Disable Time	OE to A or B	176.90	168.30	169.60	162.70	ns
t_{rA}	Input Rise Time	A port rise time	4.00	3.90	4.30	7.20	ns
t_{rB}	Input Rise Time	B port rise time	12.00	8.30	9.40	6.70	ns
t_{fA}	Input Fall Time	A port fall time	4.70	3.60	4.10	4.70	ns
t_{fB}	Input Fall Time	B port fall time	28.50	19.40	11.10	6.90	ns
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew	0.5	0.5	0.5	0.5	ns
Maximum Data Rate			40	40	40	40	Mbps

6 Electrical Specifications(Continued)

6.5 Switching Characteristics: V_{CCA}=1.8V±0.15V

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	V_{ccB}=1.8V±0.15V	V_{ccB}=2.5V±0.2V	V_{ccB}=3.3V±0.3V	V_{ccB}=5V±0.5V	Units
			Typ	Typ	Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	13.40	12.30	12.00	11.50	ns
t_{PLH}	Propagation Delay Time High-to-low Output	A to B	17.98	16.60	15.50	15.20	ns
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	13.10	11.10	10.30	9.40	ns
t_{PLH}	Propagation Delay Time High-to-low Output	B to A	18.20	15.70	15.50	13.90	ns
t_{en}	Enable Time	OE to A or B	35.80	35.80	37.10	33.60	ns
t_{dis}	Disable Time	OE to A or B	159.80	151.90	163.40	158.00	ns
t_{rA}	Input Rise Time	A port rise time	4.10	3.90	4.60	19.50	ns
t_{rB}	Input Rise Time	B port rise time	9.20	8.50	7.60	6.80	ns
t_{fA}	Input Fall Time	A port fall time	3.70	3.70	4.10	14.40	ns
t_{fB}	Input Fall Time	B port fall time	9.10	7.70	6.40	6.18	ns
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew	0.5	0.5	0.5	0.5	ns
Maximum Data Rate			50	50	50	50	Mbps

6.6 Switching Characteristics, V_{CCA}=2.5V±0.15V

over operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	V_{ccB}=2.5V±0.2V	V_{ccB}=3.3V±0.3V	V_{ccB}=5V±0.5V	Units
			Typ	Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	9.30	8.70	8.00	ns
t_{PLH}	Propagation Delay Time High-to-low Output	A to B	14.20	12.80	11.80	ns
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	9.20	7.80	7.10	ns
t_{PLH}	Propagation Delay Time High-to-low Output	B to A	13.70	12.80	11.70	ns
t_{en}	Enable Time	OE to A or B	28.70	29.35	29.80	ns
t_{dis}	Disable Time	OE to A or B	169.00	162.40	151.70	ns
t_{rA}	Input Rise Time	A port rise time	3.00	3.10	3.60	ns
t_{rB}	Input Rise Time	B port rise time	7.60	7.40	7.20	ns
t_{fA}	Input Fall Time	A port fall time	2.80	3.10	3.70	ns
t_{fB}	Input Fall Time	B port fall time	5.20	5.70	5.90	ns
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew	0.5	0.5	0.5	ns
Maximum Data Rate			70	80	80	Mbps

6 Electrical Specifications(Continued)

6.7 Switching Characteristics, V_{CCA} =3.3V±0.3V

over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	V_{ccB}=3.3V±0.3V	V_{ccB}=5V±0.5V	Units
			Typ	Typ	
t_{PHL}	Propagation Delay Time High-to-low Output	A to B	7.60	7.00	ns
t_{PLH}	Propagation Delay Time High-to-low Output	A to B	11.85	10.90	ns
t_{PHL}	Propagation Delay Time High-to-low Output	B to A	7.30	6.20	ns
t_{PLH}	Propagation Delay Time High-to-low Output	B to A	10.90	10.10	ns
t_{en}	Enable Time	OE to A or B	27.80	26.00	ns
t_{dis}	Disable Time	OE to A or B	156.90	151.90	ns
t_{rA}	Input Rise Time	A port rise time	3.10	3.20	ns
t_{rB}	Input Rise Time	B port rise time	9.20	7.30	ns
t_{fA}	Input Fall Time	A port fall time	2.90	3.20	ns
t_{fB}	Input Fall Time	B port fall time	7.40	5.40	ns
$t_{SK(O)}$	Skew(time), Output	Channel-to-Channel Skew	0.5	0.5	ns
Maximum Data Rate			80	100	Mbps

7 Typical Characteristics

T_A=25℃ (unless otherwise noted)

Parameters		Conditions		V_{CCA}							Unit
				1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
				V_{CCB}							
				5V	1.8V	1.8V	1.8V	2.5V	2.5V	3.3V to 5.5V	
				TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	Power Dissipation Capacitance	C_L=0 F=10MHz t_r=t_f=1ns OE=V_{CCA} (outputs enabled)	A-Port input B-Port output	9	8	7	8	7	8	7	pF
			B-Port input A-Port output	12	11	12	11	11	11	11	
C_{pdB}	Power Dissipation Capacitance		A-Port input B-Port output	35	26	27	27	27	27	27	
			B-Port input A-Port output	25	18	19	19	18	19	20	
C_{pdA}	Power Dissipation Capacitance	C_L=0 F=10MHz t_r=t_f=1ns OE=V_{CCA} (outputs enabled)	A-Port input B-Port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
			B-Port input A-Port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	Power Dissipation Capacitance		A-Port input B-Port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
			B-Port input A-Port output	0.01	0.01	0.01	0.01	0.01	0.01	0.01	

8 Parameter Measurement Information

Unless otherwise noted, all input pulsed are supplied by generators having the following characteristics:

- PSRR 10MHz
- Zo=50 Ω
- dv/dt ≧1V/ns

Note: All input pulses are measured one at a time with one transition per measurement

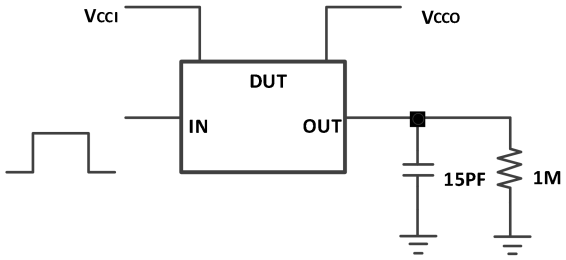


Fig.8-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise and Fall Time Measurement Using a Push-Pull Driver

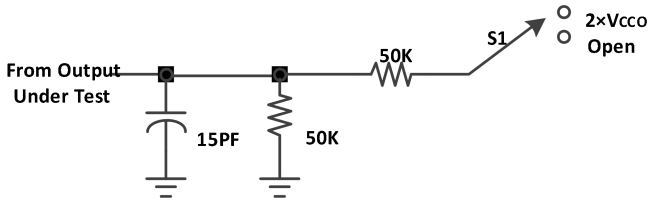


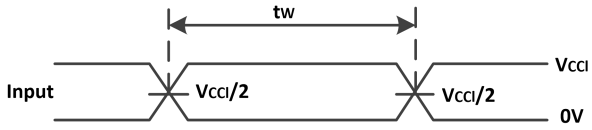
Fig.8-2. Load Circuit for Enable/Disable Time Measurement

Test	S1
t_{PZL}(1), t_{PLZ}(2)	2×V_{CCO}
t_{PHZL}(1), t_{PZH}(2)	Open

(1) t_{PZL} and t_{PZH} are the same as ten.

(2) t_{PLZ} and t_{PHZ} are the same as tdis.

8 Parameter Measurement Information(Continued)



(1) All input pulses are measured one at a time, with one transition per measurement.

Fig.8-3. Voltage Waveforms Pulse Duration

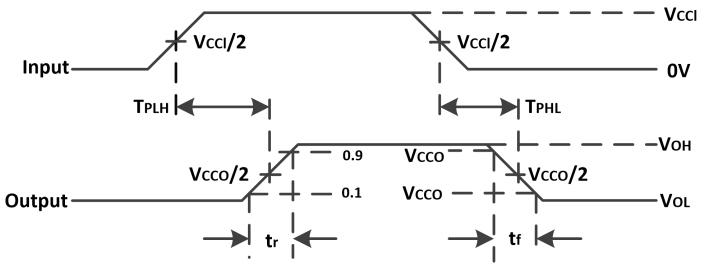


Fig.8-4. Voltage Waveforms Propagation Delay Times

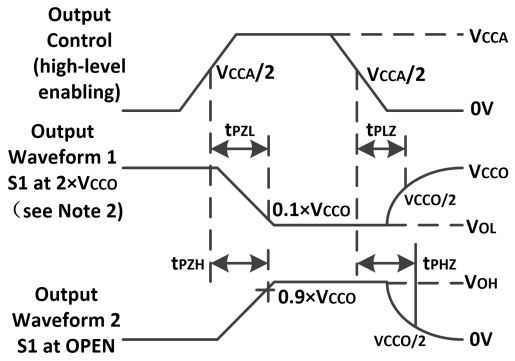


Fig.8-5. Voltage Waveforms Enable and Disable

9 Detailed Description

9.1 Overview

The GT0208 device is a 8-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 5.5 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs.

9.2 Architecture

The GT0208 device architecture does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V, and 40Ω at V_{CCO} = 3.3 V to 5 V.

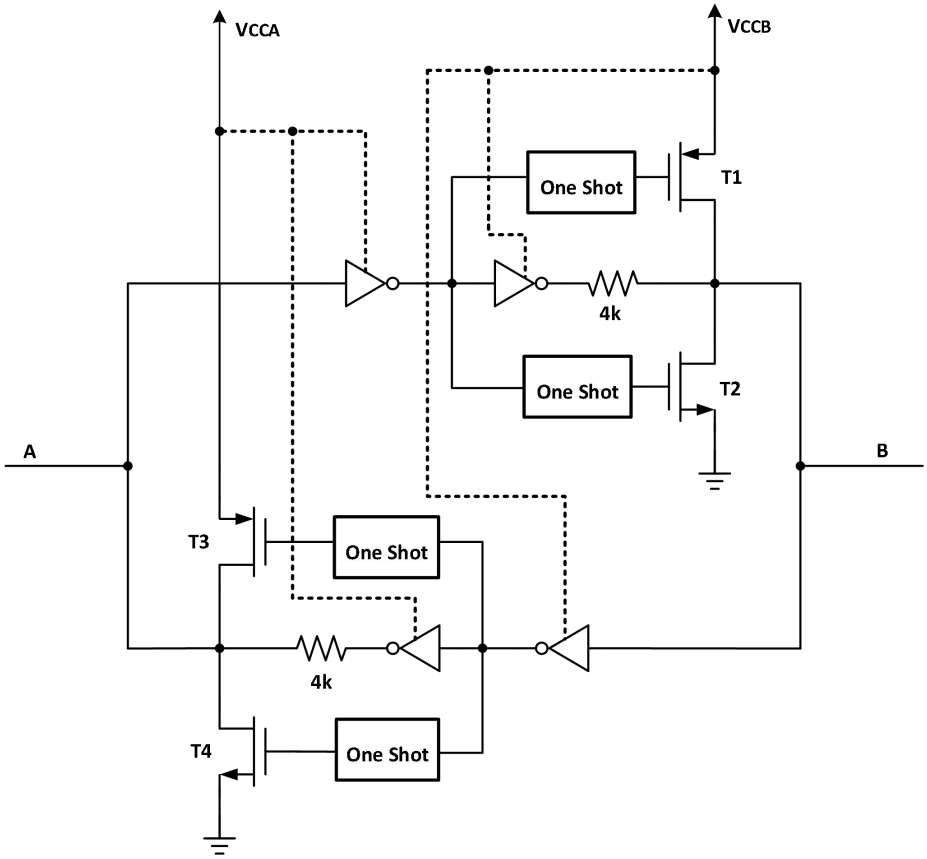
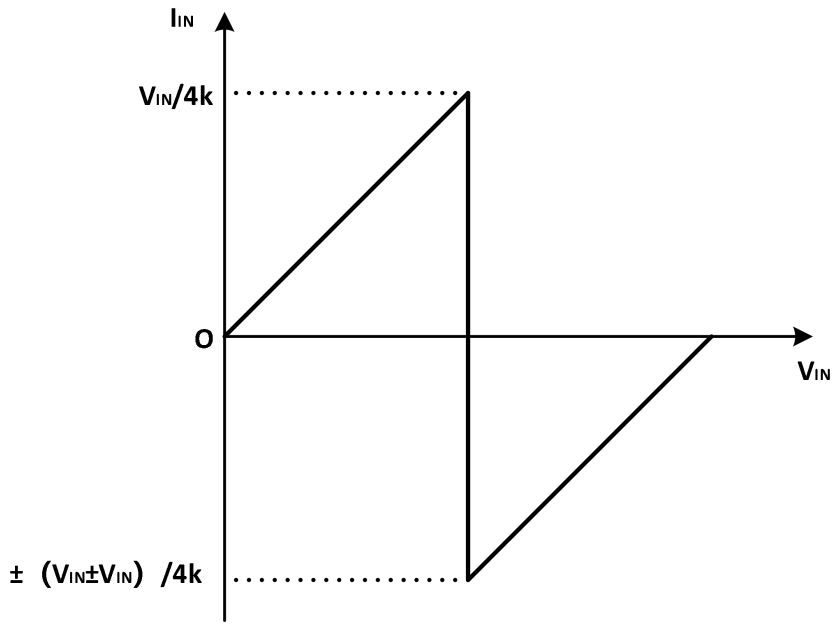


Fig.9-1. Architecture of GT0208

9 Detailed Description(Continued)

9.3 Architecture

Typical I_{IN} vs V_{IN} characteristics of the device are shown in Figure 10-2. For proper operation, the device driving the data I/Os of the GT0208 device must have driven strength of at least ±2 mA.



(1) V_T is the input threshold of the GT0208 device, (typically $V_{CC}/2$).
(2) V_D is the supply voltage of the external driver.

Fig. 9-2. Typical I_{IN} vs V_{IN} Curve

9.4 Output Load Considerations

We recommend careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

9.5 Enable and Disable

The GT0208 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (ten) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

9 Detailed Description(Continued)

9.6 Pullup or Pulldown Resistors on I/O Lines

The device is designed to drive capacitive loads of up to 70 pF. The output drivers of the GT0208 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the GT0208 device. For the same reason, the GT0208 device must not be used in applications such as I^2C or 1-Wire where an open drain driver is connected on the bidirectional data I/O. For these applications, use a device from the GT010X series of level translators.

9.7 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

10 Application Information

The GT0208 device can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I^2C or 1-wire, where the data is bidirectional and no control signal is available. The device can also be used in applications where a push-pull driver is connected to the data I/Os, but the GT0208 might be a better option for such push-pull applications.

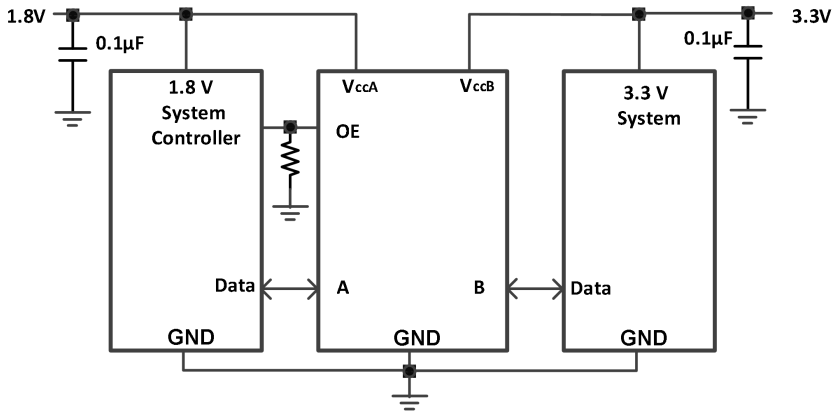
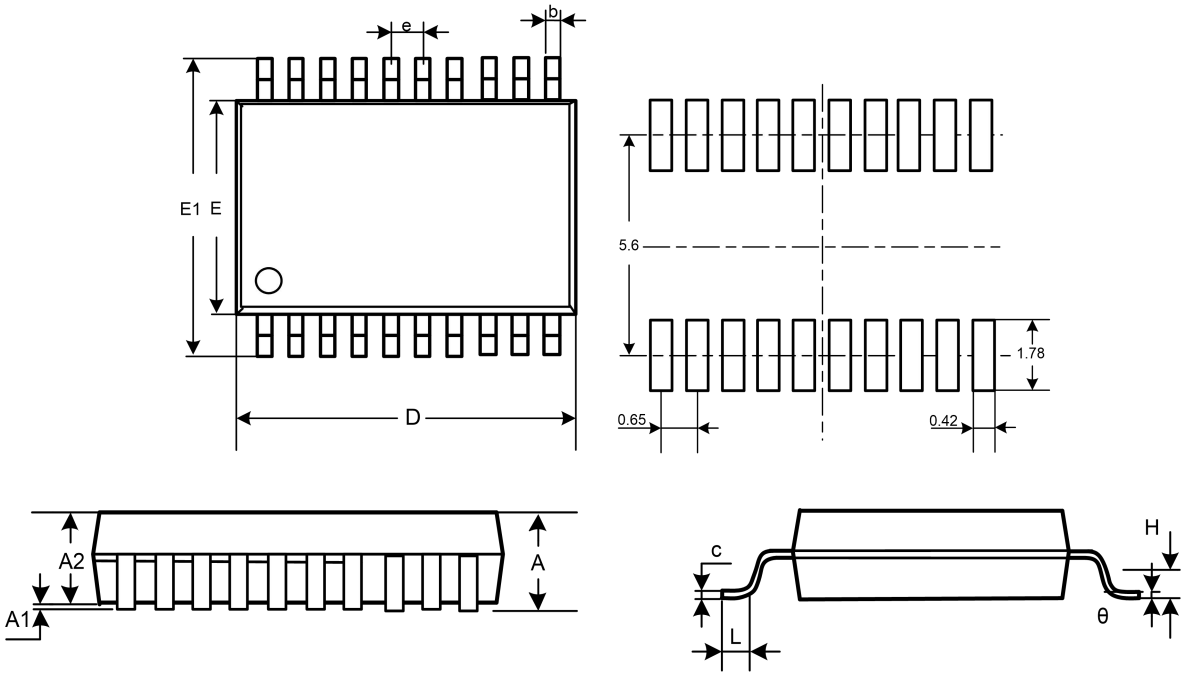


Fig.10-1. Typical Application Schematic

11 Package Outline Dimension

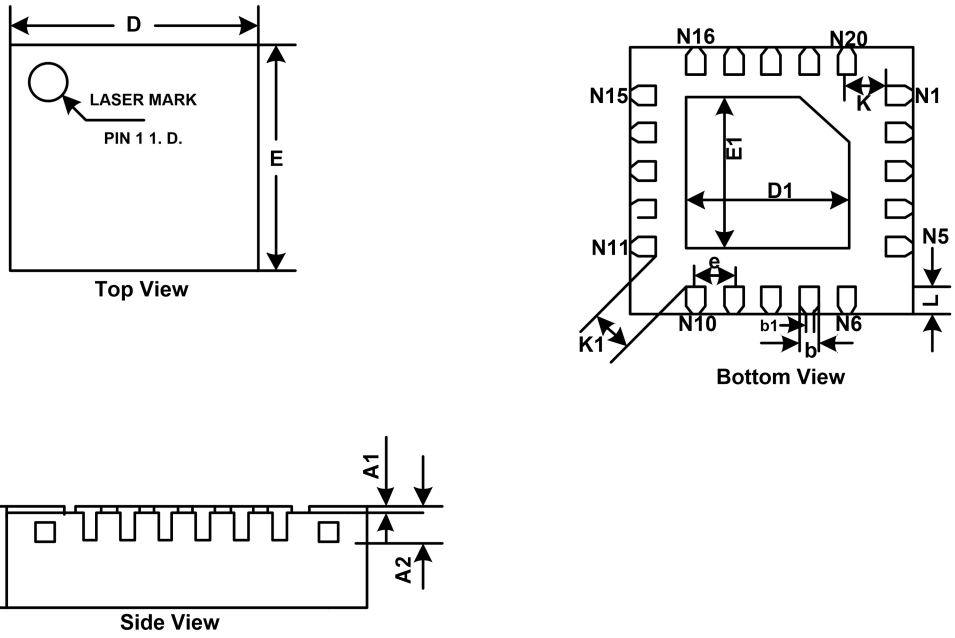
TSSOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.200	0.280	0.008	0.011
c	0.130	0.170	0.005	0.007
D	6.400	6.600	0.252	0.260
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.65BSC		0.026BSC	
L	0.450	0.750	0.018	0.030
H	0.25TYP		0.01TYP	
θ	0°	8°	0°	8°

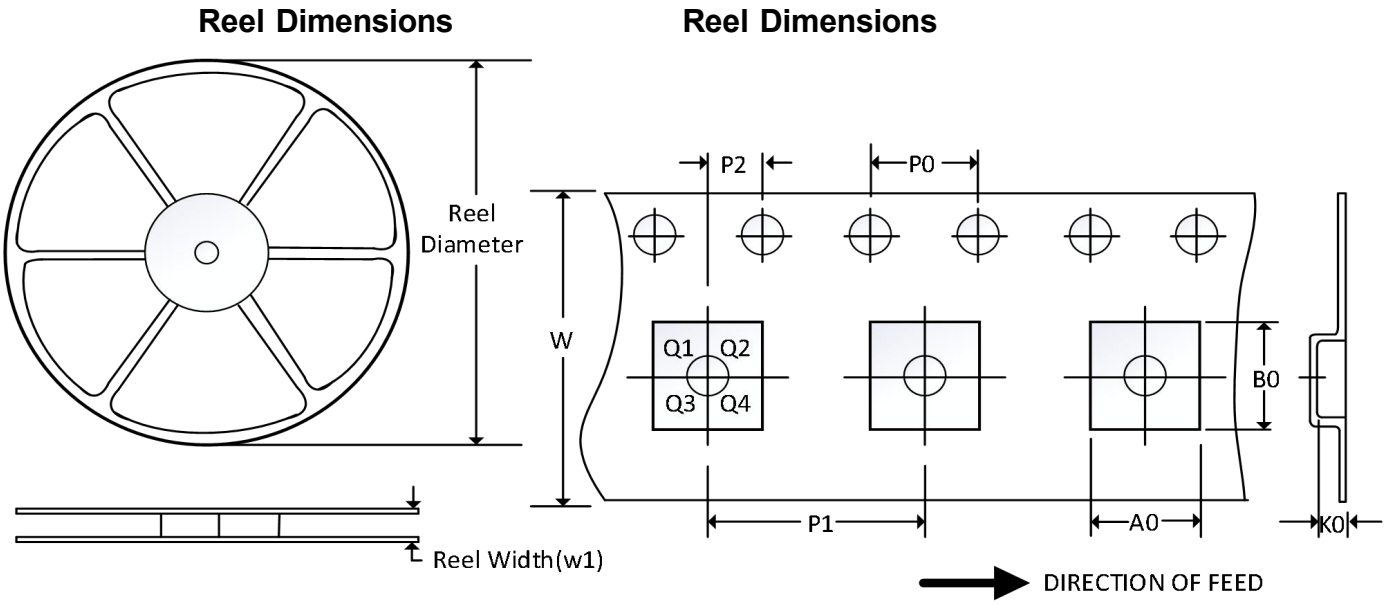
11 Package Outline Dimension(Continued)

QFN3×3-20L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203REF		0.008REF	
D	2.950	3.050	0.116	0.120
E	2.950	3.050	0.116	0.120
D1	1.550	1.650	0.061	0.065
E1	1.550	1.650	0.061	0.065
K	0.300REF		0.012REF	
K1	0.400REF		0.016REF	
b	0.150	0.250	0.006	0.010
b1	0.150REF		0.006REF	
e	0.400BSC		0.016BSC	
L	0.350	0.450	0.014	0.018

12 Tape and Reel Information



Note: The picture is only for reference. Please make the object as the standard.

Key Parameter List of Tape and Reel

Package type	Reel diameter	Reel width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 QµAdrant
TSSOP20	13''	12.4	6.75	6.95	1.20	4.0	8.0	2.0	12.0	Q1
QFN3X3-20L	13''	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

Note:
(1)All dimensions are nominal.
(2)Plastic or metal protrusions of 0.15mm maximum per side are not included.