GT74LVC86A
Quadruple 2-Input Exclusive-OR Gate

1 Features	2 Application
- Supports 5V V_{CC} operation - Inputs accept voltages to 5.5V - Max t_{pd} of 6ns at 3.3 V - Low power consumption, 10μA max I_{CC} - ±24-mA output drive at 3.3V - I_{off} supports partial-power-down mode	- Wireless headsets - Motor drives and controls - TVs - Set-top boxes - Audio

3 Description

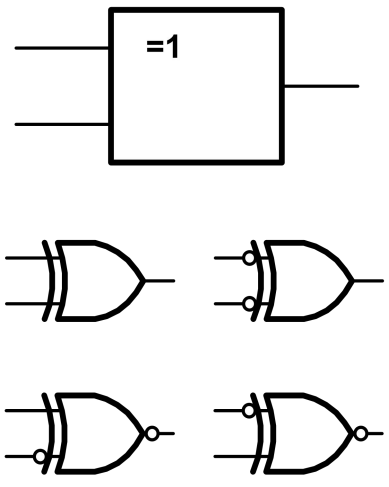
This quadruple 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

The GT74LVC86A performs the Boolean function $Y=A \oplus B$ or $Y=\bar{A}B+A\bar{B}$ in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Circuit Diagram



4 Revision History

Revision	Date	Note
Rev. A0. 0	2023. 09. 02	Original Version
Rev. A0. 1	2023. 12. 26	1.Updated Package Qty 2.Added Tape and Reel Information 3.Added Marking 4.Added MSL
Rev. A1. 0	2024. 04. 11	1.Updated Electrical Specifications 2.Added Typical Characteristics

The latest datasheet version should be checked on the GTIC official website, as the company does not actively inform customers about updates to the datasheet.

5 Device Summary, Pin and Packages

Table. 5-1. Device Summary(1)

Serial Name	Part Name	Package	Body Size (Nom)	Marking(2)	MSL(3)	Package Qty
GT74LVC86A	GT74LVC86APD	SOP14	8.65mm×3.90mm×1.75mm	GT74LVC86A XXXXXXX	3	Tape and Reel,4000
	GT74LVC86ATD	TSSOP14	5.00mm×4.40mm×1.20mm	GT74LVC86A XXXXXXX	3	Tape and Reel,4000

(1) For all available packages, please contact product sales.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

(4) "XXXXX" in Marking will be appeared as the batch code.

5 Device Summary, Pin and Packages(Continued)

Top View

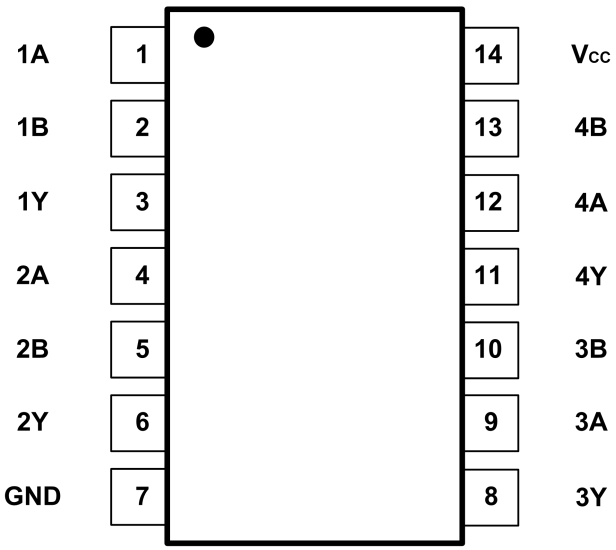


Fig.5-1. GT74LVC86A: PD (SOP14) Package
GT74LVC86A: TD (TSSOP14) Package

Table. 5-2. Pin Definition

Pin		I/O	Description
Name	PD TD		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1Y	3	O	Channel 2, Output Y
2A	4	I	Channel 2, Input A
2B	5	I	Channel 2, Input B
2Y	6	O	Channel 2, Output Y
3A	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
3Y	8	O	Channel 3, Output Y
4A	12	I	Channel 4, Input A
4B	13	I	Channel 4, Input B
4Y	11	O	Channel 4, Output Y
V_{CC}	14	-	Positive Supply
GND	7	-	Ground

6 Voltage, Temperature, ESD and Thermal Ratings

6.1 Absolute Maximum Ratings

Parameters			Min.	Max.	Unit
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range		-0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range		-55	150	℃
T_{stg}	Storage temperature		-55	150	℃

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

ESD			Value	Unit
V(ESD)	Electrostatic discharge	Human-body model (HBM)	8 K	V
		Charged-device model (CDM)	1.25 K	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6 Voltage, Temperature, ESD and Thermal Ratings(Continued)

6.3 Recommended Operating Conditions(1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_{IH}	High-Level Input Voltage	V_{CC}=1.65V to1.95V	0.65×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
V_{IL}	Low-Level Input Voltage	V_{CC}=1.65V to1.95V		0.35×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
I_{OL}	Low-Level output Current	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Δt/Δv	Input Transition Rise or Fall Rate	V_{CC}=1.8V±0.15V,2.5V±0.2V		20	ns/V
		V_{CC}=3.3V±0.3V		10	
		V_{CC}=5V±0.5V		5	
TA	Operating Free-air Temperature	All Other Packages	40	125	°C

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6.4 Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP14	180	35	°C/W
SOP14	120	36	°C/W

7 Electrical Specifications

7.1 Electrical Characteristics

FULL=–40°C to +125°C, Typical values are at TA=+25°C. (unless otherwise noted)

Parameters	Symbol	Conditions	V_{CC}	T_A	Min.	Typ.	Max.	Unit
Output								
High-Level Output Voltage	V_{OH}	I_{OH}=–100μA	1.65V to 5.5V	FULL	V_{CC}-0.1			V
		I_{OH}=–4mA	1.65		1.2			
		I_{OH}=–8mA	2.3		1.9			
		I_{OH}=–16mA	3		2.4			
		I_{OH}=–24mA			2.3			
		I_{OH}=–32mA	4.5		3.8			
Low-Level Output Voltage	V_{OL}	I_{OL}=100μA	1.65V to 5.5V	FULL			0.1	V
		I_{OL}=4mA	1.65				0.45	
		I_{OL}=8mA	2.3				0.3	
		I_{OL}=16mA	3				0.4	
		I_{OL}=24mA					0.55	
		I_{OL}=32mA	4.5				0.55	
Off-State Current	I_{off}	V_I or V_O=5.5V	0V	FULL			±10	μA
Input								
Input Leakage Current	I_I	A or B input, V_I=5.5V or GND	0V to 5.5V	FULL			±5	μA
Input Capacitance	C_i	V_I=V_{CC} or GND	3.3V	FULL		6		pF
Power Supply								
Power Supply Range	V_{CC}		1.65V to 5.5V	FULL	1.65		5.5	V
Supply Current	I_{CC}	V_I=5.5 V or GND, I_O=0	1.65V to 5.5V	FULL			10	μA
Delta Power Current	ΔI_{CC}	One Input at V_{CC} – 0.6 V, Other Inputs at V_{CC} or GND	3V to 5.5V	FULL			500	μA

(1) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

7.2 Switching Characteristics

Over recommended operating free-air temperature range,C_L=30pF or 50 pF (unless otherwise noted)

Parameter	From(Input)	To(Output)	–40°C to +125°C								Units
			V_{CC}=1.8V±0.15V		V_{CC}=2.5V±0.2V		V_{CC}=3.3V±0.3V		V_{CC}=5V±0.5V		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	3.5	12	1.8	7	1.3	6	1	5	ns

7.3 Operating Characteristics

TA=–40°C to +125°C

Parameter		Test Conditions	V_{CC}=1.8V	V_{CC}=2.5V	V_{CC}=3.3V	Units
			Typ	Typ	Typ	
C_{pd}	Power Dissipation Capacitance	f=10Mhz	20	20	20	pF

8 Typical Characteristics

Typical values are at TA=+25°C (unless otherwise noted)

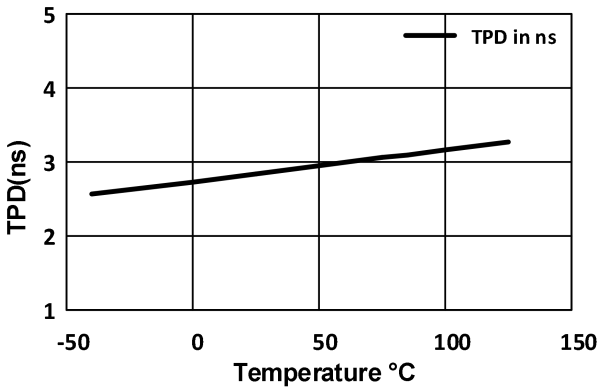


Fig.8-1. TPD Across Temperature at 3.6V V_{CC}

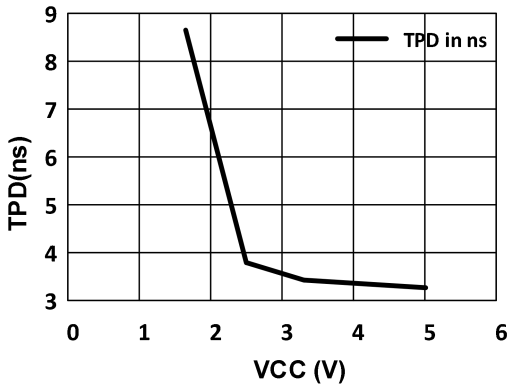
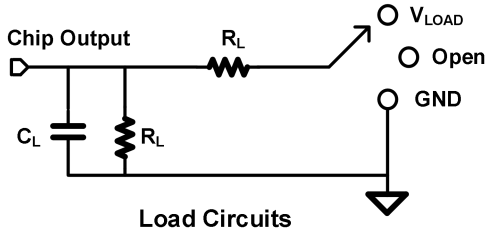


Fig.8-2. TPD Across V_{CC} at 25℃

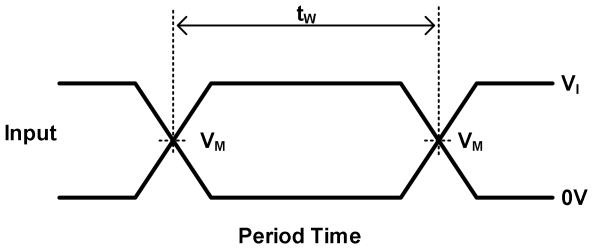
9 Measurement Information



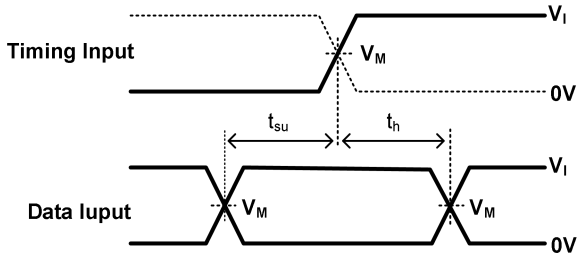
Load Circuits

TEST	S1
T_{PHL}/T_{PLH}	OPEN
T_{PLZ}/T_{PZL}	V_{LOAD}
T_{PHZ}/T_{PZH}	GND

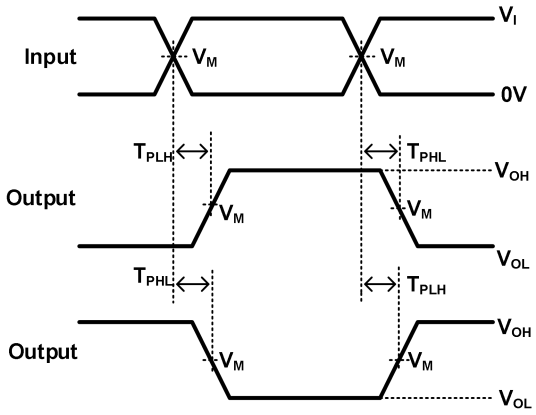
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	T_r/T_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
2.5V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1MΩ	0.15V
3.3V±0.15V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.15V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	15pF	1NΩ	0.3V



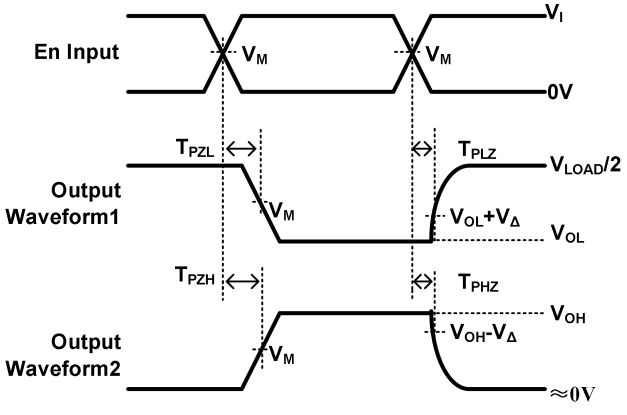
Period Time



Setup and Hold Times



Propagation Delay
for Output and Inverted Output



Enable and Disable Times
Low-And High-Level Enabling

Notes: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 .
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
F. t_{PZL} and t_{PZH} are the same as t_{en} .
G. t_{PLH} and t_{PHL} are the same as t_{pd} .
H. All parameters and waveforms are not applicable to all devices.

10 Detailed Description

The GT74LVC86A device performs the Boolean function $Y=\bar{A}B+A\bar{B}$ in positive logic. This quadruple 2-input exclusive-OR gate is designed for 1.65V to 5.5V V_{CC} operation.

A common application is as a true and complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Table.10-1. Function Table

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

11 Application Note

The GT74LVC86A device can accept input voltages up to 5.5 V at any valid Vcc which makes the device suitable for down translation. This feature of the GT74LVC86A makes it ideal for various bus interface applications.

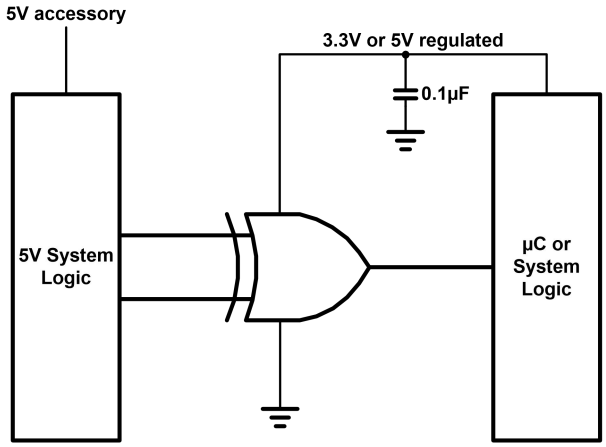
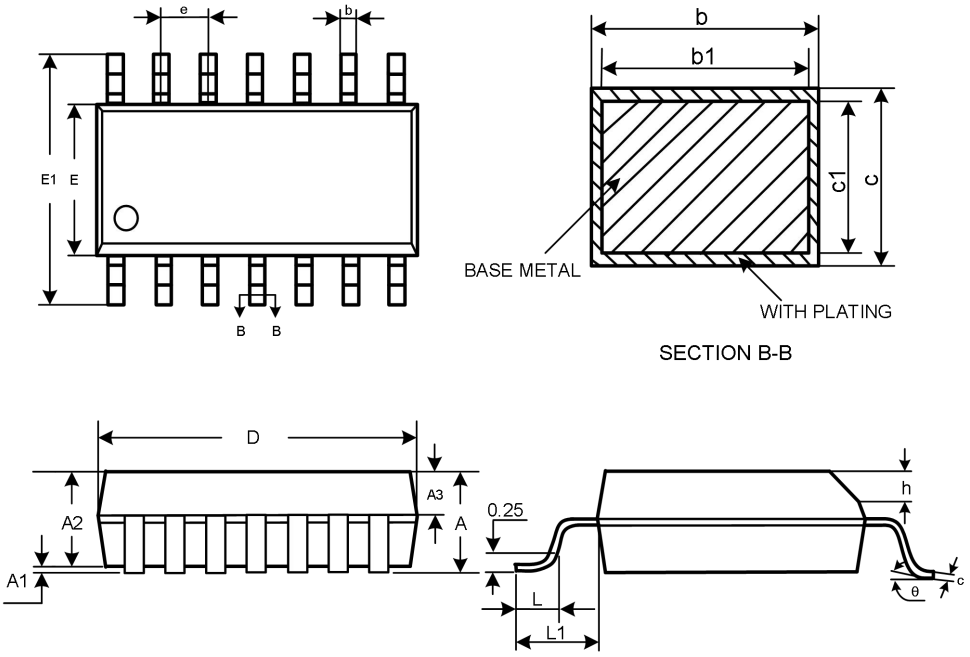


Fig.11-1. Typical Application Schematic

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

12 Package Outline Dimension

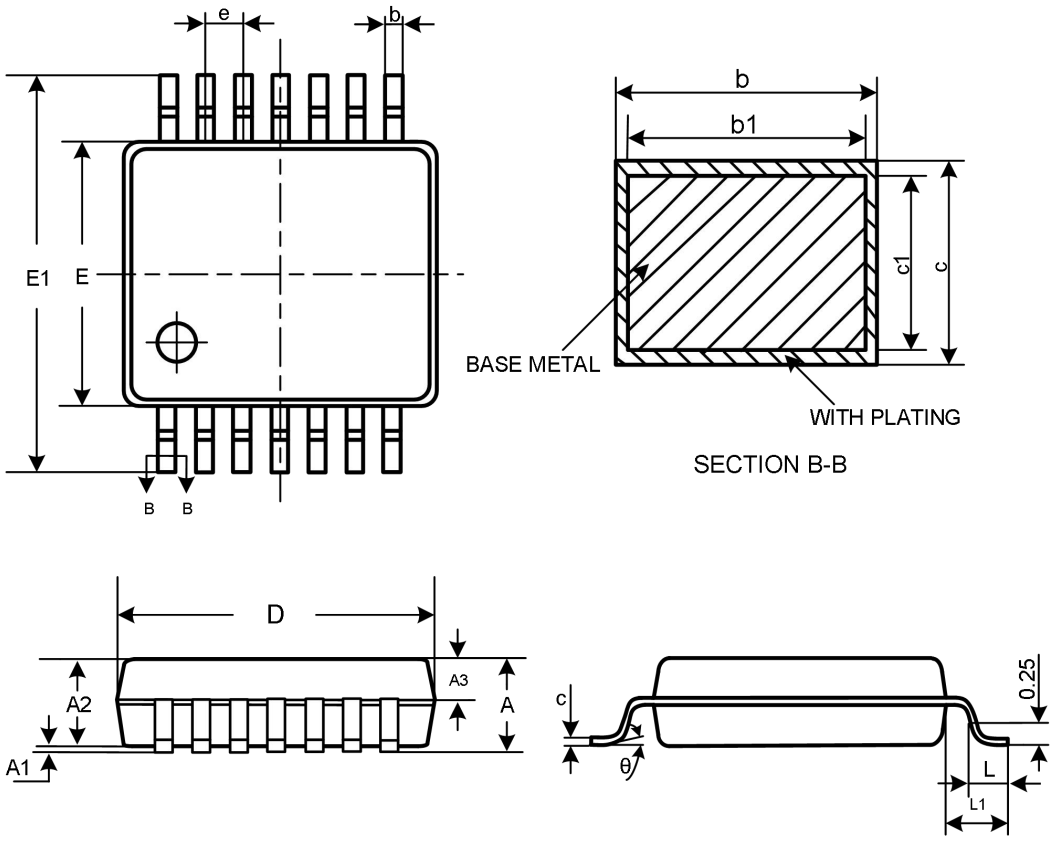
SOP14



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	——	——	1.75
A1	0.10	——	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	——	0.47
b1	0.38	0.41	0.44
c	0.20	——	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E1	5.80	6.00	6.20
E	3.80	3.90	4.00
e	1.27BSC		
h	0.25	——	0.50
L	0.50	——	0.80
L1	1.05REF		
θ	0°	——	8°

12 Package Outline Dimension(Continued)

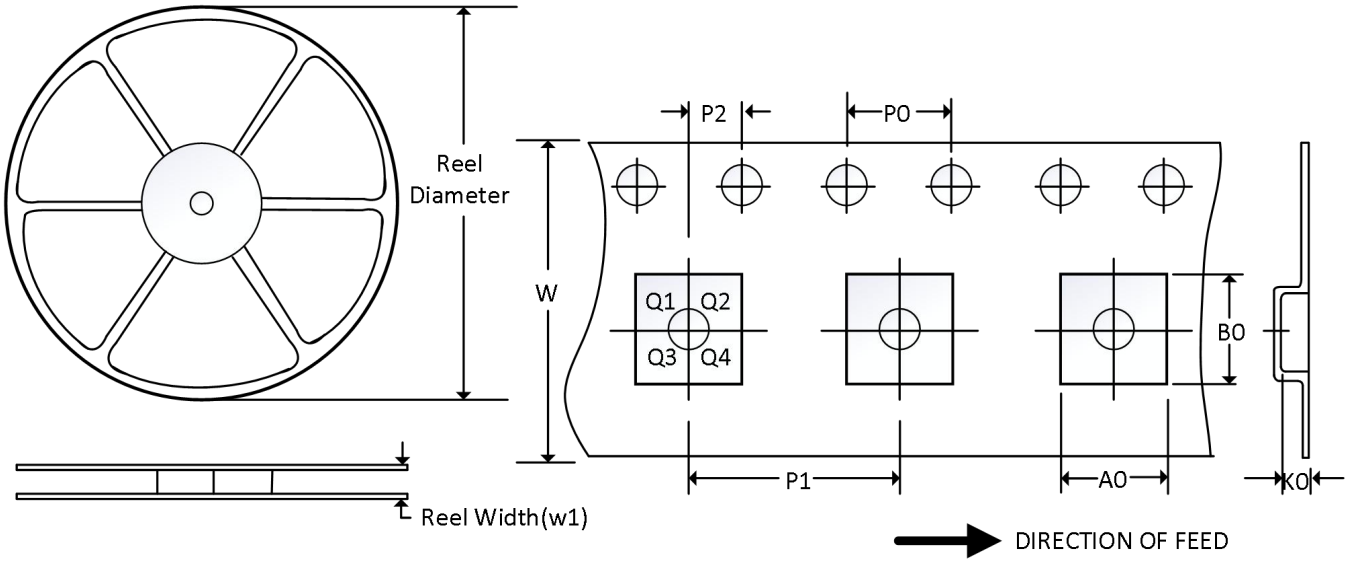
TSSOP14



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	——	——	1.20
A1	0.05	——	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	——	0.28
b1	0.19	0.22	0.25
c	0.13	——	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BCS		
θ	0°	——	8°

13 Tape and Reel Information

Reel Dimensions **Reel Dimensions**



NOTE: The picture is only for reference. Please make the object as the standard.

Key Parameter List of Tape and Reel

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP14	13''	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
SOP14	13''	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.